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Jameco Part Number 43297

Rockwell

R6532
RAM-I/O-Timer (RIOT)

DESCRIPTION

The R6532 RAM-I/O-Timer (RIOT) integrates random access memory (RAM), parallel I/O data ports and timer functions into a single peripheral device which operates in conjunction with any CPU in the R6500 microprocessor family. It is comprised of a 128 × 8 static RAM, two software-controlled, 8-bit bidirectional data ports allowing direct interfacing between the microcomputer and peripheral devices, a software programmable interval timer, with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect circuit.

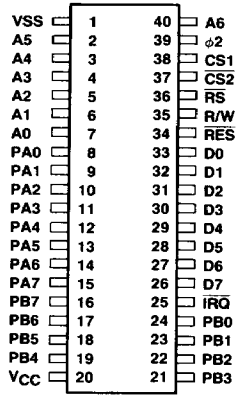
FEATURES

- 128 × 8 static RAM
- Two 8 bit bidirectional data ports
- Programmable interval timer with interrupt capability
- TTL & CMOS compatible peripheral lines
- One port has direct transistor drive capability
- Programmable edge-sensitive interrupt input
- 8 bit bidirectional data bus
- 6500/6800 bus compatible
- 1 MHz and 2 MHz parts available
- Single +5V power supply

ORDERING INFORMATION

Part Number: R6532 _ _ _

- Temperature Range:
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Package:
  - C = Ceramic DIP
  - P = Plastic DIP
- Frequency:
  - No Letter = 1 MHz
  - A = 2 MHz



R6532 Pin Configuration

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INTERFACE SIGNALS

RESET ($\overline{RES}$)

During system initialization, a low $\overline{RES}$ input causes a zeroing of all four I/O registers. This in turn causes all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least two clock periods when reset is required.

READ/WRITE (R/$\overline{W}$)

The R/$\overline{W}$ signal is supplied by the microprocessor and controls the transfer of data to and from the R6532. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the data supplied by the R6532. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the R6532.

INTERRUPT REQUEST ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interrupt control logic. The pin will be normally high with a low indicating an interrupt from the R6532. An external 3K pull-up resistor is required. The $\overline{IRQ}$ pin may be activated by a transition on PA7 or timeout of the interval timer.

DATA BUS (D0–D7)

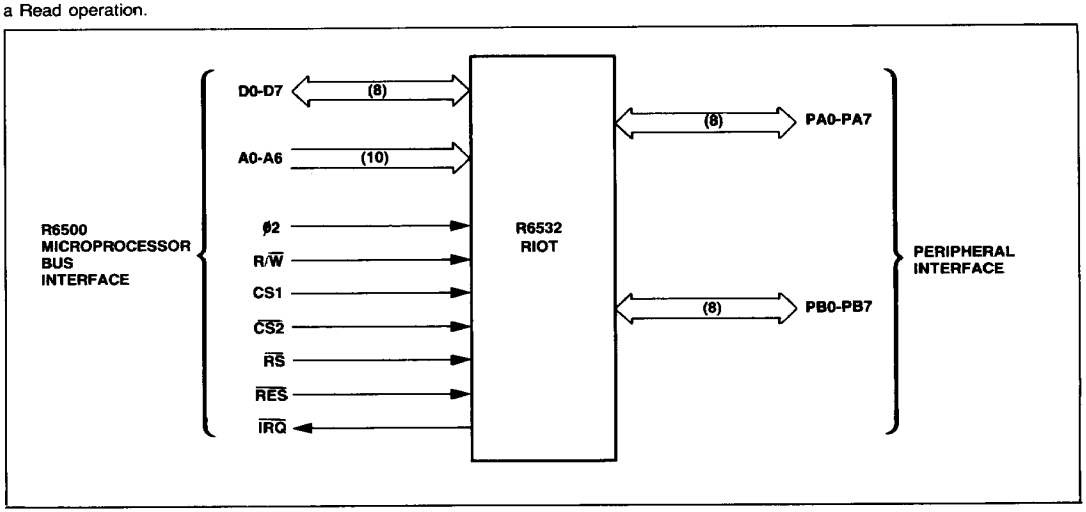
The R6532 has eight bidirectional data pins (D0–D7). These pins connect to the system's data lines and transfer data between the R6532 and the microprocessor data bus. The output buffers remain off, or tri-stated, except when the R6532 is selected for a Read operation.

ADDRESS LINES (A0–A6)

There are seven address pins (A0–A6). In addition, there is the $\overline{RAM\ SELECT}$ ($\overline{RS}$) pin. The pins A0–A6 and $\overline{RS}$ are always used as addressing pins. There are two additional pins which are used as CHIP SELECTS. They are pins CS1 and $\overline{CS2}$. Tables 1 and 2 identify the functions selected and registers addressed depending upon the address line and $\overline{RS}$ inputs in conjunction with the R/$\overline{W}$ level.

I/O PORTS (PA0–PA7, PB0–PB7)

The R6532 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0–PA7 and PB0–PB7. (PA7 also has another use which is discussed later.) Each is set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" written into the data direction register causes its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and the internal pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor reads the peripheral pin. When the peripheral device gets information from the R6532 it receives data stored in the data register. The microprocessor reads valid pin information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volt for a "0" as the peripheral pins are all TTL compatible. Pins PB0–PB7 are also capable of sourcing 3 ma at 1.5V, thus making them capable of Darlington drive.



RIOT Interface Signals

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Table 1. Address Decoding

Operation	$\overline{RS}$	R/$\overline{W}$	A4	A3	A2	A1	A0
Write RAM	0	0	—	—	—	—	—
Read RAM	0	1	—	—	—	—	—
Write Output Reg A	1	0	—	—	0	0	0
Read Output Reg A	1	1	—	—	0	0	0
Write DDRA	1	0	—	—	0	0	1
Read DDRA	1	1	—	—	0	0	1
Write Output Reg B	1	0	—	—	0	1	0
Read Output Reg B	1	1	—	—	0	1	0
Write DDRB	1	0	—	—	0	1	1
Read DDRB	1	1	—	—	0	1	1
Write Timer							
÷1T	1	0	1	(a)	1	0	0
÷8T	1	0	1	(a)	1	0	1
÷64T	1	0	1	(a)	1	1	0
÷1024T	1	0	1	(a)	1	1	1
Read Timer	1	1	—	(a)	1	—	0
Read Interrupt Flag	1	1	—	—	1	—	1
Write Edge Detect Control	1	0	0	—	1	(b)	(c)

Notes:
— = Don't Care, "1" = High level (≥2.4V), "0" = Low level (≤0.4V)

(a) A3 = 0 to disable timer interrupt
A3 = 1 to enable timer interrupt

(b) A1 = 0 to disable PA7 interrupt
A1 = 1 to enable PA7 interrupt

(c) A0 = 0 for negative edge-detect
A0 = 1 for positive edge-detect

Table 2. Register Addressing

Start Address +	Register/Function	Start Address +	Register/Function
$0	DRA ('A' side data register)	$7	Write edge-detect control (positive edge-detece, enable interrupt)
$1	DDRA ('A' side data direction register)		
$2	DRB ('B' side data register)	$C	Read timer (enable interrupt)
$3	DDRB ('B' side data direction register)	$14	Write timer (divide by 1, disable interrupt)
$4	Read timer (disable interrupt)	$15	Write timer (divide by 8, disable interrupt)
$4	Write edge-detect control (negative edge-detect, disable interrupt)	$16	Write timer (divide by 64, disable interrupt)
		$17	Write timer (divide by 1024, disable interrupt)
$5	Read interrupt flag register (bit 7 = timer, bit 6 = PA7 edge-detect) Clear PA7 flag	$1C	Write timer (divide by 1, enable interrupt)
		$1D	Write timer (divide by 8, enable interrupt)
$5	Write edge-detect control (positive edge-detect, disable interrupt)	$1E	Write timer (divide by 64, enable interrupt)
		$1F	Write timer (divide by 1024, enable interrupt)
$6	Write edge-detect control (negative edge-detect, enable interrupt)		

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INTERNAL ORGANIZATION

The R6532 is divided into four basic sections, RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and a Data Register (DR).

RAM—128 BYTES (1024 BITS)

The 128 × 8 Read/Write Memory acts as a conventional static RAM and can be accessed from the microprocessor by selecting the chip (CS1 = high, $\overline{CS2}$ = low) and by setting $\overline{RS}$ low. Address lines A0 through A6 then select the desired byte of storage.

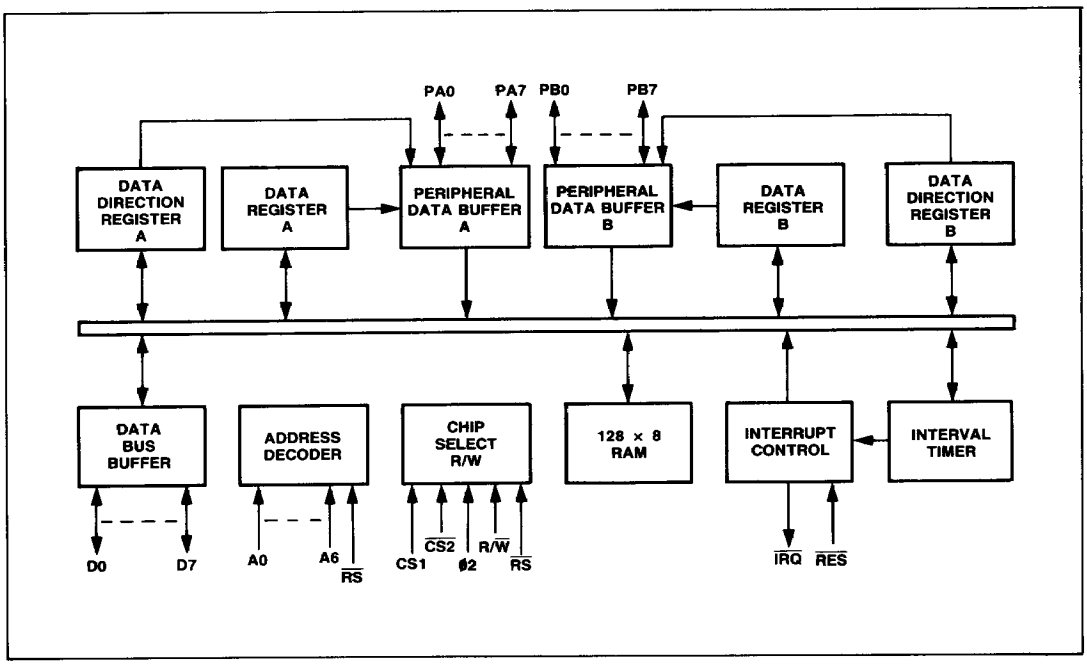
I/O PORTS AND REGISTERS

The I/O Ports consist of eight lines which can be individually programmed to act as either an input or an output. A logic zero in a bit of the Port A Data Direction Register (DDRA) causes the corresponding line of Port A to act as an input. A logic one causes the corresponding Port A line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Port A Data Register (DRA).

Data is read directly from the data pins during any read operation. For any output pin, the data transferred into the processor will be the same as that contained in the Data Register if the voltage on the pin is allowed to go to 2.4V for a logic one. Note that for input lines, the processor can write into the corresponding bit of the Data Register. This will not affect the polarity on the pin until the corresponding bit of DDRA is set to a logic one to allow the I/O line to act as an output.

The operation of the Port B is exactly the same as the normal I/O operation of the Port A. Each of the eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Port B Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin is controlled by the Port B Data Register (DRB).

The primary difference between Port A and the Port B is in the operation of the output buffers which drive these pins. The Port B output buffers are push-pull devices which are capable of sourcing 3 ma at 1.5V. This allows these pins to directly drive transistor switches. To assure that the microprocessor will read proper data on a "Read Port B" operation, logic in the R6532 allows the microprocessor to read the Output Register instead of reading the peripheral pin as on Port A.



R6532 Block Diagram

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EDGE DETECTING WITH PA7

In addition to acting as a peripheral I/O line, the PA7 line can be used as an edge-detecting input. In this mode, an active transition sets the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag causes $\overline{IRQ}$ output to go low if the PA7 interrupt has been enabled.

Control of the PA7 edge detecting mode is accomplished by writing to one of four addresses. In this operation, A0 controls the polarity of the active transition and A1 acts to enable or disable interrupting of the processor. The data which is placed on the Data Bus during this operation is discarded and has no effect on the control of PA7.

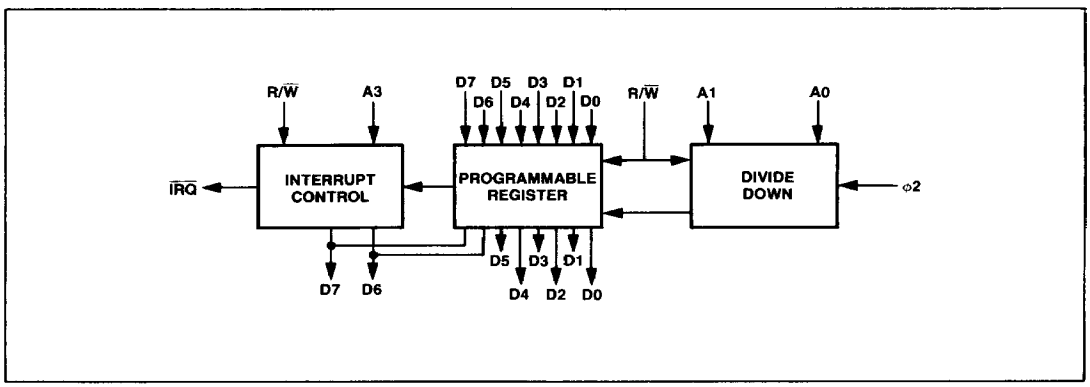
The PA7 interrupt flag is set on an active transition, even if the pin is being used as a normal input or as a peripheral control output. The flag is also set by an active transition if the PA7 interrupt is disabled. The reset signal ($\overline{RES}$) disables the PA7 interrupt and enables negative (high-to-low) edge detection on PA7. The PA7 edge detect logic can be set to detect either a positive or negative transition and to either enable or disable interrupt ($\overline{IRQ}$) generation upon detection.

During system initialization, the interrupt flag may inadvertently be set by an unexpected transition on the PA7. It is therefore recommended that the interrupt flag be cleared *before* enabling interrupting from PA7. To clear PA7 interrupt flag, simply read the interrupt Flag Register.

INTERVAL TIMER

The Timer section of the R6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic.

The Timer can be programmed to count up to 255 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to logic "1". After the interrupt flag is set the internal clock begins counting down at the system clock rate to a maximum of −255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.



Basic Elements of Interval Timer

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INTERVAL TIMER EXAMPLE

The 8-bit microprocessor data bus transfers data to and from the Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the data bus and written into the divide by 1 Timer register.

At the same time that data is being written to the Timer, the counting intervals of 1, 8,64, 1024T are decoded from address lines A0 and A1. During a Read or Write Operation address line A3 controls the interrupt enable, i.e., A3 = 1 enables $\overline{IRQ}$, A3 = 0 disables $\overline{IRQ}$. When the time is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

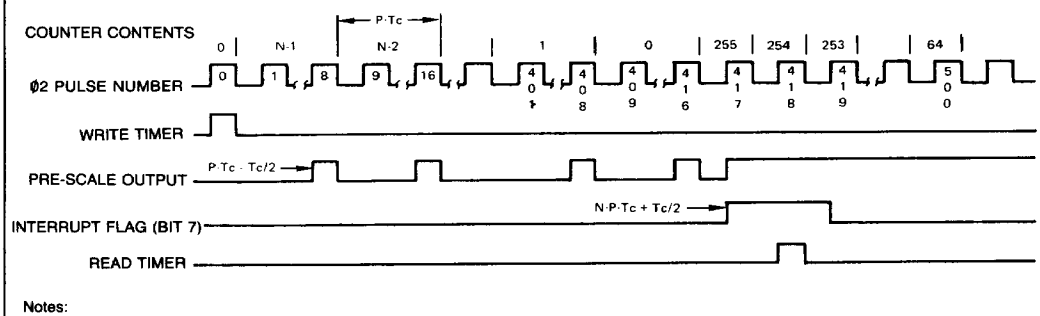
When the Timer has counted through 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After the interrupt flag is set, the timer register decrements at a divide by "1" rate of the system clock. If the timer is read after the interrupt flag is set and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in two's complement, but remember that interrupt occurred on count number one. Therefore, we must subtract 1.

Value read	= 1 1 1 0 0 1 0 0	
Complement	= 0 0 0 1 1 0 1 1	
ADD 1	= 0 0 0 1 1 1 0 0 =	28 Equals two's complement of register
SUB 1	= 0 0 0 1 1 0 1 1 =	27

Thus, to arrive at the *total* elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 × 8) + 1 = 417T. Total elapsed time would be 416T + 27T = 443T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

The interrupt flag will be reset whenever the Timer is accessed by a read or a write. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flags are read (D7 for the timer, D6 for the edge detect) data bus lines D0–D5 go to 0.

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.



Notes:
Assume 52 Loaded into Timer with a divide by 8.
The Counter Contents and the Clock Pulse Numbers will coincide.
Prescale, P = 8.
Cycle Time, T_C = 1 μsec (for 1 MHz)
Count, N = 52

Interval Time Example Waveforms

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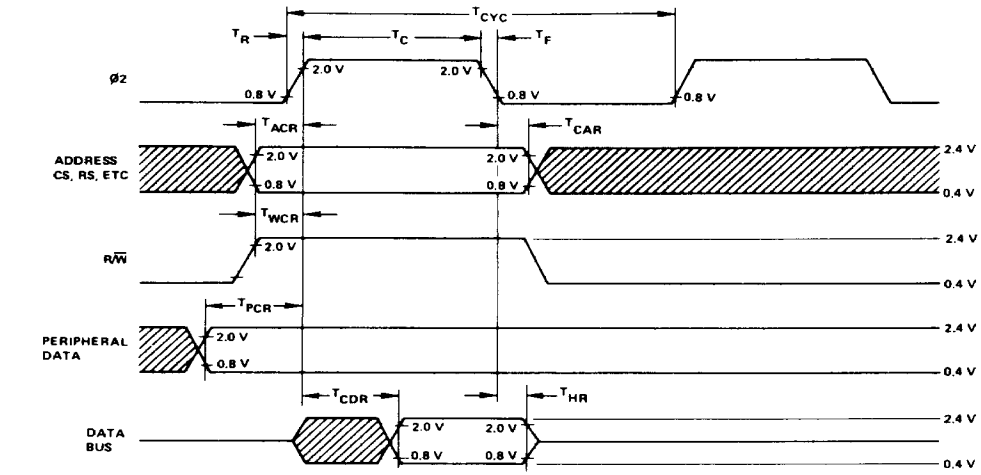
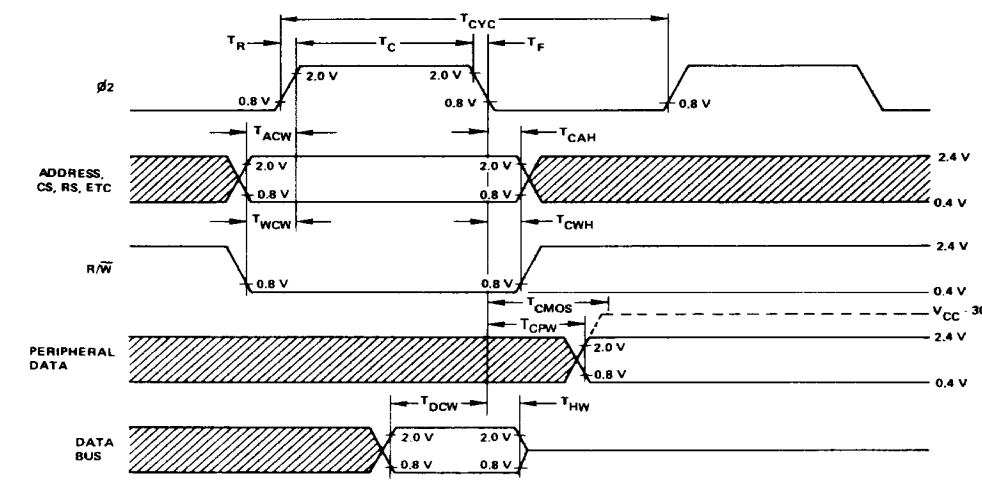
BUS AND PERIPHERAL TIMING WAVEFORMS

READ TIMING



WRITE TIMING



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AC CHARACTERISTICS

Characteristic	Symbol	R6532 (1 MHz) Min	R6532 (1 MHz) Max	R6532A (2 MHz) Min	R6532A (2 MHz) Max	Unit
Clock Cycle Time	T_{CYC}	1	10	0.5	10	μs
Clock Pulse Width	T_C	470	—	240	—	ns
Rise & Fall Times	T_R, T_F	—	25	—	15	ns

READ TIMING

Address Set Up Time	T_{ACR}	180	—	90	—	ns
Address Hold Time	T_{CAR}	0	—	0	—	ns
R/$\overline{W}$ Set Up Time	T_{WCR}	180	—	90	—	ns
Data Bus Delay Time	T_{CDR}	—	395	—	190	n
Data Bus Hold Time	T_{HR}	10	—	10	—	ns
Peripheral Data Set Up Time	T_{PCR}	300	—	150	—	ns

WRITE TIMING

Ø2 Cycle Time	T_{CYC}	1	10	0.5	10	μs
Ø2 Pulse Width	T_C	470	—	240	—	ns
Address Set Up Time	T_{ACW}	180	—	90	—	ns
Address Hold Time	T_{CAH}	0	—	0	—	ns
R/$\overline{W}$ Set Up Time	T_{WCW}	180	—	90	—	ns
R/$\overline{W}$ Hold Time	T_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	T_{DCW}	300	—	150	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns
Peripheral Data Delay Time	T_{CPW}	—	1	—	0.5	μs
Peripheral Data Delay Time CMOS	T_{CMOS}	—	2	—	1	μs

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MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	 °C °C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0 ±5%, T_A = T_L to T_H unless otherwise noted)

Parameter	Symbol	Min	Max	Unit[1]	Test Conditions
Input High Voltage	V_{IH}	2.4	V_{CC}	V	
Input Low Voltage	V_{IL}	0	0.4	V	
Input Leakage Current: A0-A6, RS, R/$\overline{W}$, $\overline{RES}$, Ø2, CS1,$\overline{CS2}$	I_{IN}	—	2.5	µA	V_{IN} = 5.25V V_{CC} = 0V
Input Leakage Current for Three-State Off D0-D7	I_{TSI}	—	±10	µA	V_{IN} = 0.4V to 2.4V
Input High Current PA0-PA7, PB0-PB7	I_{IH}	−100	—	µA	V_{IH} = 2.4V
Input Low Current PA0-PA7, PB0-PB7	I_{IL}	—	−1.6	mA	V_{IN} = 0.4V
Output High Voltage PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7 (other than TTL drive, e.g., Darlington)	V_{OH}	 2.4 1.5	 — —	V	V_{CC} = 4.75V I_{LOAD} = −100 µA I_{LOAD} = 3 mA
Output Low Voltage D0-D7	V_{OL}	—	0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7 (other drive, e.g., Darlington)	I_{OH}	 −100 −3.0	—	 µA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking) PA0-PA7, PB0-PB7	I_{OL}	1.6	—	mA	V_{OL} = 0.4V
Input Capacitance Ø2 Other	 C_{CLK} C_{IN}	 — —	 30 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	10	pF	
Power Dissipation	P_D	—	1000	mW	T_A = 0°C

Notes:
1. All units are direct current (DC).
2. Negative sign indicates outward current flow, positive indicates inward flow.

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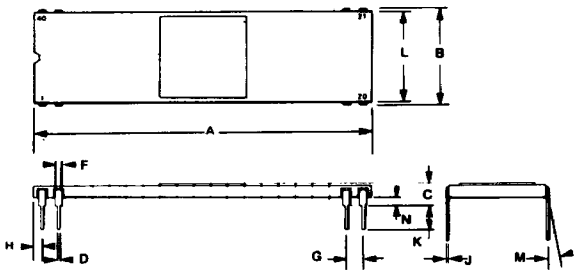
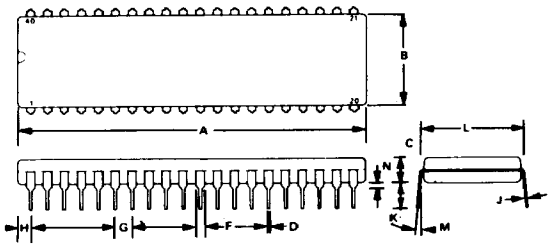
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

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